REMARKS

Applicant respectfully requests favorable reconsideration of this application.

Claims 105-118 and 130-143 are pending. Claims 1-104 and 119-129 were previously cancelled without prejudice or disclaimer.

In the Office Action, Claim 108 was rejected under 35 U.S.C. § 112, first paragraph; and Claims 105-118 and 130-143 were rejected under 35 U.S.C. § 102(e) over Schubert (U.S. 2003/0069724A, hereinafter "Schubert").

Rejection Under 35 U.S.C. § 112, First Paragraph

In the Office Action, Claim 8 was rejected under 35 U.S.C. § 112, first paragraph, for allegedly containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, to make and/or use the invention. More specifically, the Office alleges that there is no description in the specification of what makes a connection "incompatible". Applicant respectfully disagrees.

"Incompatible connections" as recited in Claim 108 is described in detail in various portions of Applicant's disclosure. For example:

> "[0037] According to another characteristic of the method, the data processing system compares the physical connections between the components to the connection coherency rule table, in order to detect any incompatibilities between the ends of the connections between the components, and in such a case, it specifies, and adds into the instance connection table, an adapter component inserted into the connection in question."
>
> "[0095] The description of the rules for interconnecting the components...can exist in the form of at least one table. In the exemplary embodiment of Fig.6, it is shown in the form of seven associated...tables.... .This table represents the rules for generating connections between signals".

> "[0079] The concepts of interfaces and ports are used to support the description of connections between the components".
>
> "[0080] ...[A] port is an arbitrary selection of signals of the HDL-type interface of a component. A given signal can belong to one or more ports. The definition of each port is constituted by pairs of regular expressions and corresponding substitute expressions. These expressions are successively applied to the name of each signal of the interface, and in case an appropriate "match", the substitute expression is applied... . If the final substitution gives a final result that is identical for two signals, the latter will be connected to one another. The configurator generates a unique name for the connection and places the appropriate information in the wiring table (TCAB). The method described makes it possible to express complex connection rules between the components. For example, it is possible to connect signals with different names, or to create rules for connecting the input signals with the output signals".
>
> "[0084] The Configurator system analyzes the connections of the composite model components and searches for sharable interface adapters at the level of common ports. If there is no suitable component with which to share the connection by observing the signals, an interface adapter component...will be instantiated...".

Paragraphs [0037], [0074], [0079], [0080, [0084], and [0090] of Applicant's published application (as amended by the Preliminary Amendment of December 15, 2003) (underlines added).

As the above-noted portions of Applicant's disclosure make clear, the components are connected based on specific rules, as shown in Fig. 6, for example. The Configurator generates a unique name for each connection, which makes it possible to connect signals with different names or to create rules for connecting input signals to output signals. The Configurator also analyzes the connections by observing the signals, and, if there is no suitable component with which to share the connection, an interface adapter component is instantiated. Therefore, it is clear from Applicant's disclosure that components are interconnected based on specific rules, and further, that a connection is "incompatible" if the Configurator determines based

on the signals (signal names, signal input output connections), that there is no suitable component with which to share the connection based on these interconnection rules.

Therefore, Applicant respectfully submits that the claimed "incompatible connections" are sufficiently described in Applicant's disclosure so as to enable one skilled in the art to make and use the claimed invention of Claim 108.

In view of the foregoing, Applicant respectfully submits that Claim 108 and all other claims containing this limitation are sufficiently described in Applicant's disclosure so as to enable one skilled in the art to make and use Applicant's claimed invention. See MPEP §§ 2164.01 and 2164.04; *In re Bowen*, 492 F.3d 859, 862-63 (CCPA 1974).

Accordingly, Applicant respectfully requests that the rejection under § 112 be withdrawn.

Rejection Under 35 U.S.C. § 102

Claims 105-118 and 130-143 were rejected under 35 U.S.C. § 102 over Schubert. This rejection is respectfully traversed.

Claims 105 and 130 recite a computer system and method for automatically generating a simulation model for a selected configuration of software simulation elements, comprising, *inter alia*, automatically generating source code files comprising the simulation model corresponding to the selected configuration specified by the configuration definition file, and in which the simulation model comprises software simulation elements each corresponding to an integrated circuit which together comprise the design of a processing machine that conforms to a functional specification of the selected configuration as defined in the configuration definition file. Support is provided, for example, at paragraphs [0053] through

[0056], [0081] through [0094], [0114], and [0141] of Applicants' disclosure. It is apparent that the applied reference does not teach or suggest at least these features.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." See MPEP § 2131.0 and *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, "[t]he identical invention must be shown in as complete detail as is contained in the ...claim". See *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Here, it appears that several limitations recited in Claims 105 and 130 are entirely missing from the applied reference. For example, while the Office Action lists paragraphs from Schubert which allegedly include teachings relevant to Claim 105 and 130, Applicant respectfully submits that the cited portions of Schubert do not teach or suggest at least the following limitations from Claims 105 and 130, nor does the Office Action specifically point out which elements in Schubert correspond to and perform the same function as the claimed elements. For example, none of the paragraphs cited by the Office Action are understood as teaching or suggesting "creating a simulation wiring", or "using the configuration definition file, a component and connection rule table, and a connection coherency rule table for simulating at least one of the plurality of integrated circuits", or "automatically generating source code files comprising the simulation model corresponding to the selected configuration specified by the configuration definition file, wherein the simulation model comprises software simulation elements corresponding to an integrated circuit".

Furthermore, it is apparent that the only paragraph in Schubert that mentions "simulation model" is paragraph [0142], which recites that "[t]he DIC HDL

description 318 can be utilized by a functional simulator or synthesis and place & route tools. The instrument or 322 can also produce an optional DIC simulation model 322 that permits functional simulation of the instrumented description 316". However, contrary to the assertions made in the Office Action, there is no further teaching or suggestion in any of the cited paragraphs as to how the simulation model is generated or used, storing of simulation elements, creating simulation wirings, or generating source code files comprising the simulation model. Therefore, Schubert is not understood as teaching or suggesting the subject matter of Claims 105 and 130.

Moreover, Schubert fails to teach or suggest a system and process for automatically generating a simulation model for a selected configuration of software simulation elements, as claimed. Schubert discloses in paragraphs [0011] – [0013] that functional simulation and formal verification are two electronic system debugging and verification techniques that have the disadvantage of needing simulation models and needing generating of simulation models. Schubert therefore, uses a different technique to debug and diagnose HDL-based electronic systems, which system apparently does not need generating simulations models. *See*, for example, paragraph [0024]. As such, it is apparent that Schubert teaches away from the claimed system and process for automatically generating a simulation model for selected configuration software simulation elements. Moreover, Schubert does not teach or suggest at least "creating a simulation wiring", or "using the configuration definition file, a component and connection rule table, and a connection coherency rule table for simulating at least one of the plurality of integrated circuits", or "automatically generating source code files comprising the simulation model corresponding to the selected configuration specified by the configuration definition

file, wherein the simulation model comprises software simulation elements corresponding to an integrated circuit, as claimed in Claims 105 and 130.

Therefore, Applicant respectfully submits that Claims 105 and 130 distinguish patentably from the applied reference.

Claims 106-118 and 131-143 are also believed to be patentable based on their dependence from Claims 105 and 130, respectively, as well as due to the additional subject matter recited in Claims 106-118 and 131-143.

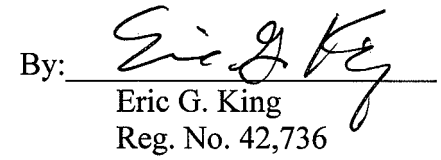
In view of the foregoing, Applicant respectfully submits that this application is in condition for allowance. Accordingly, a prompt Notice of Allowance is respectfully solicited.

However, should the Examiner believe that any further action is necessary to place this application in better form for allowance, the Examiner is invited to contact Applicant's representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2147-908626) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

Date: December 1, 2008

By: 

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